REMARKS

Claims 10-17, 19, 25-34 and 38-52 are pending in the Application. Claims 10-13 are allowed. Claims 14-17, 19, 25-34, 38-52 are rejected under 35 U.S.C. §102(e). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

Applicants thank the Examiner for discussing the Office Action with Applicants' attorney on December 15, 2005. Upon discussing the Office Action with the Examiner, Applicants enclose herewith further arguments to more particularly point out why Applicants believe that the rejections are in error.

The Examiner is reminded that the Examiner must respond to each argument presented below pursuant to M.P.E.P. §707.07(f).

I. REJECTIONS UNDER 35 U.S.C. §102(e):

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Cheong does not disclose "setting a predetermined data value in a first portion of a preselected first queue entry in a queue operable for storing a plurality of instructions for issuing to an instruction unit" as recited in claim 14. The Examiner cites column 7, lines 1-27 and column 10, lines 48-51 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse and assert that Cheong instead discloses that Figure 3 depicts a table for tracking the source data required by a dispatched instruction. Column 10, lines 48-49. Cheong further discloses that the table tracks whether the source data is available and holds the data until the instruction is issued. Column 10, lines 49-51. Hence, Cheong discloses a table that tracks the source data required by dispatched instructions. There is no language in the cited passages that discloses setting a predetermined data value. Neither is there any language in the cited

passages that discloses setting a predetermined data value in a first portion of a preselected queue entry. Neither is there any language in the cited passages that discloses setting a predetermined data value in a first portion of a preselected queue entry in a queue operable for storing a plurality of instructions. Neither is there any language in the cited passages that discloses setting a predetermined data value in a first portion of a preselected queue entry in a queue operable for storing a plurality of instructions for issuing to an instruction unit. Thus, Cheong does not disclose all of the limitations of claim 14, and thus Cheong does not anticipate claim 14. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "said queue including a plurality of entries, each entry being associated with an instruction for issuing, wherein said first queue entry is preselected in response to a first data value in a second portion of a preselected second queue entry" as recited in claim 14. The Examiner cites to Figure 3 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse. The Examiner has not identified which element in Figure 3 allegedly discloses a first queue entry. Neither has the Examiner identified which element in Figure 3 allegedly discloses a first data value. Neither has the Examiner identified which element in Figure 3 allegedly discloses a second portion of a preselected second queue entry. Applicants respectfully request the Examiner to identify such elements in Figure 3 pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 14, and thus Cheong does not anticipate claim 14. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein the first portion comprises a link mask" as recited in claim 14. The Examiner cites elements 118, 128a, 128b and column 8, lines 23-36 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse. Cheong instead discloses that the (Target Identification) TID field 118 contains the TID which was assigned to the dispatched instruction. Column 11, lines 5-6. Cheong further discloses that element 128a corresponds to the source TID field. Column 11, lines 40-42. Cheong further discloses that element 128b stores data. Column 11, lines 18-

20. Cheong further discloses that the processor is provided with a target identification ("TID") generator which generates tokens, or tags, each of which is uniquely associated with an instruction upon dispatch. Column 8, lines 31-34. Cheong further discloses that the TIDs are used to retain program order information and track data dependencies. Column 8, lines 34-36. Hence, Cheong discloses generating tokens, each of which is associated with an instruction upon dispatch. Cheong further discloses that target identifications are used to retain program order and track data dependencies. The Examiner has not identified which of the cited elements correspond to a first portion. Further, if the Examiner is identifying a TID as being a link mask, the Examiner must provide a basis in fact and/or technical reasoning to support such an interpretation. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). While the Examiner may interpret terms broadly, claims are not to be read in a vacuum and must be interpreted in light of the specification. *In re Marosi*, 710 F.2d 799, 802 (Fed. Cir. 1983); M.P.E.P. §2111.01. Applicants had previously discussed on pages 14-15 of Paper No. 4, the specification in connection with the term "link mask". The Examiner appears to ignore such passages of the Specification and instead equate her own interpretation to "link mask" not in light of the specification and then conclude that Cheong discloses a link mask. Paper No. 5, page 11. This is entirely improper. As a result, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 14. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "selecting for issuing an instruction associated with said entry containing said predetermined data value in said first portion in response to said predetermined data value" as recited in claim 14. The Examiner cites column 10, lines 48-51 and column 11, lines 27-34 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 4. Applicants respectfully traverse and assert that Cheong instead discloses that Figure 3 depicts a table for tracking the source data required by a dispatched instruction. Column 10, lines 48-49. Cheong further discloses that the table tracks whether the source data is available and holds the data until the instruction is issued. Column 10, lines 49-51. Cheong further discloses that to illustrate the operation of the PEQ, it will be assumed that only one source register is required by the instruction associated with the PEQ

entry. Column 11, lines 27-29. Cheong further discloses that the source needed bit for source block one is set and the source needed bit source block two is low. Column 11, lines 29-31. Cheong further discloses that if the valid/tagged field 124a indicates that the data in value field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. Column 11, lines 31-34. Hence, Cheong discloses a table that tracks the source data required by dispatched instructions. Cheong further discloses that if the data in field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. While Cheong discloses issuing an instruction if the data in field 126a is valid, the Examiner has not identified with specificity in Cheong which element discloses the first portion of the preselected first queue entry. Is the Examiner asserting that element 126a is the first portion? Is the Examiner asserting that element 126a is the entry containing the predetermined data value? Is the Examiner asserting that the data in field 126a is a predetermined data value? Applicants respectfully request the Examiner to more particularly point out which elements in Cheong allegedly disclose the above-cited claim limitations. Thus, Cheong does not disclose all of the limitations of claim 14, and thus Cheong does not anticipate claim 14. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "a dispatch unit coupled to said input means" as recited in claim 29. The Examiner cites elements 1024, 1026, 1032 and column 6, lines 5-17 of Cheong as disclosing input means. Paper No. 5, page 5. The Examiner further cites element 1220 and column 7, lines 50-51 of Cheong as disclosing a dispatch unit. Applicants respectfully traverse. Cheong instead discloses that element 1024 corresponds to a keyboard; element 1026 corresponds to a mouse and element 1032 corresponds to a track ball. Column 6, lines 5-17. These are input devices that allow the user to input to the computer system. Further, Cheong discloses that element 1220 corresponds to a dispatch unit in a processor. Column 7, lines 50-51. However, a person skilled in the art would not consider that these input devices (e.g., mouse) are coupled to dispatch unit 1220. Further, the Examiner has not provided a basis in fact and/or technical reasoning to support the assertion that a person skilled in the art would interpret a mouse or other such input devices as communicating a plurality of instructions. *See Ex parte Levy*,

17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990); *In re Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2d 1949, 1950-51 (Fed. Cir. 1999). The Examiner cannot read the claims in a vacuum but must interpret the claims in light of the specification. *In re Marosi*, 710 F.2d 799, 802 (Fed. Cir. 1983); M.P.E.P. §2111.01. Thus, Cheong does not disclose all of the limitations of claim 29, and thus Cheong does not anticipate claim 29. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "each execution unit including a self-initiated instruction issue mechanism for receiving said instructions and issuing instructions to an execution logic circuit for execution" as recited in claim 29. The Examiner cites elements 1222, 1228 and 1230 as disclosing execution units. Paper No. 5, page 5. The Examiner further cites column 7, lines 50-54 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 5. Applicants respectfully traverse and assert that Cheong instead discloses that the dispatch unit 1220 decodes and dispatches one or more instructions from instruction queue 1219 to execution units 1222, 1228 and 1230. Column 7, lines 51-54. While Cheong does disclose dispatching instruction to execution units from the dispatch unit, the Examiner has not shown where Cheong discloses that each execution unit (1222, 1228 and 1230) includes a self-initiated instruction issue mechanism for receiving the instruction and issuing instructions to an execution logic for execution. The Examiner cannot ignore claim language. All words in a claim must be considered in judging the patentability of that claim against the prior art. *See In re Wilson*, 424 F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Thus, Cheong does not disclose all of the limitations of claim 29, and thus Cheong does not anticipate claim 29. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "said queue including a plurality of entries, each queue entry having a first portion and second portion, said first portion operable for storing a link data value, said first portion comprising a link mask and said first link data value indicating to a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy" as recited in claim 29. The Examiner cites Figure 3, elements 118, 128a, 128b, 124a,

124b, 126a, 126b as well as column 8, lines 23-62 and column 11, lines 31-45 of Cheong as disclosing the above-cited claim limitations. Paper No. 5, page 5. Applicants respectfully traverse and assert that Cheong instead discloses that the processor is provided with a target identification ("TID") generator which generates tokens or tags, each of which is uniquely associated with an instruction upon dispatch. Column 8, lines 31-34. Cheong further discloses that if the valid/tagged field 124a indicates that the data in valid field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. Column 11, lines 31-34. Cheong further discloses that in the illustrative embodiment of the invention, the execution unit broadcast their results along with the TID of the instruction which generated them. Column 11, lines 38-40. Cheong further discloses that when a TID being broadcast matches the TID value in the source TID field 128a, the GPR value being broadcast is copied into value field 126a and the valid/tagged field 124a is set to indicate valid. Column 11, lines 40-44. There is no language in the cited passages that discloses that each queue entry has a first portion and a second portion. The Examiner has not identified with particularity where Figure 3 discloses a queue entry that has a first portion and a second portion. Where is the first portion? Where is the second portion? Further, there is no language in the cited passages that discloses that the first portion is operable for storing a link data value. The Examiner has not identified where Cheong discloses a link data value. Further, there is no language in the cited passages that discloses a first portion comprising a link mask. The Examiner has not identified where Cheong discloses a link mask. Further, there is no language in the cited passages that discloses a first portion including the link data value indicating to a target instruction which of the queue's plurality of entries that a dispatching dependent instruction will occupy. Applicants respectfully request the Examiner to more particularly point out which elements in Cheong allegedly disclose each of the above-cited claim limitations pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 29, and thus Cheong does not anticipate claim 29. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "said second portion operable for storing a first data value, and wherein said first data value in a first queue

entry is set in response to a first link data value in a preselected second queue entry" as recited in claim 29. The Examiner cites elements 126a, 126b and column 11, lines 4-20 and 31-45 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 5. Applicants respectfully traverse and assert that Cheong instead discloses that if the valid/tagged field 124a indicates that the data in valid field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. Column 11, lines 31-34. Cheong further discloses that in the illustrative embodiment of the invention, the execution unit broadcast their results along with the TID of the instruction which generated them. Column 11, lines 38-40. Cheong further discloses that when a TID being broadcast matches the TID value in the source TID field 128a, the GPR value being broadcast is copied into value field 126a and the valid/tagged field 124a is set to indicate valid. Column 11, lines 40-44. There is no language in the cited passage that discloses a second portion operable for storing a data value. Neither is there any language in the cited passage that discloses a second portion operable for storing a data value where the data value is set in response to a link data value in a preselected second queue entry. Applicants respectfully request the Examiner to particularly identify in Figure 3 which element allegedly discloses a queue entry with a second portion where that second portion is operable for storing a data value where the data value is set in response to a link data value in a preselected second queue entry pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 29, and thus Cheong does not anticipate claim 29. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "a rename register device coupled to said queue, said rename register device including a plurality of entries, each entry having a first portion operable for storing a pointer data value and a second portion operable for storing a validity data value, wherein each pointer data value is associated with a corresponding queue entry, and wherein each first link data value is set in response to said pointer data values and said validity data values" as recited in claim 29. The Examiner cites elements 1233 and 1237 of Cheong as disclosing a rename register device. Paper No. 5, page 6. The Examiner further cites element 1219 of Cheong as disclosing a queue. Paper No. 5, page 6. The Examiner

further cites column 9, lines 37-48 as disclosing a rename register device including a plurality of entries. Paper No. 5, page 6. The Examiner further cites elements 104 and 102 of Cheong for the phrase beginning with "each entry having a first portion" and ending with the phrase "validity data value." Paper No. 5, page 6. The Examiner further cites column 9, line 49 – column 10, line 3 of Cheong as disclosing that each pointer data value is associated with a corresponding queue entry. Paper No. 5, page 6. The Examiner further cites column 10, lines 40-47 of Cheong as disclosing that each first link data value is set in response to the pointer data values and the validity data values. Paper No. 5, page 6. Applicants respectfully traverse.

Cheong instead discloses that the GPR table comprises a plurality of entries, each entry being associated with a particular architectural register. Column 9, lines 39-41. Cheong further discloses that there are 32 entries, one for each general purpose register available in the exemplary PowerPC architecture. Column 9, lines 41-43. Cheong further discloses that each entry in the GPR table consists of four fields: valid/tagged field 100, value field 102, TID field 104 and a field to provide compression of history buffer entries. Column 9, line 49 – column 10, line 5. Cheong further discloses that the valid/tagged field 112, value field 114, and TID field 116 all contain data related to the architected register targeted by the dispatched instruction. Column 10, lines 40-42. Cheong further discloses that Figure 3 depicts a table for tracking the source data required by a dispatched instruction. Column 10, lines 48-49. There is no language in the cited passages that discloses that each entry of the rename register device (Examiner asserts that elements 1233, 1237 disclose a rename register device) has a first portion operable for storing a pointer data value. The Examiner has not shown an entry in element 1233 that has a first portion operable for storing a pointer data value. Further, there is no language in the cited passages that discloses that each pointer data value is associated with a corresponding queue entry. Neither is there any language in the cited passages that discloses a link data value set in response to the pointer data values. Neither is there any language in the cited passages that discloses a link data value set in response to the pointer data values and validity data values. Thus, Cheong does not disclose all of the limitations of claim 29, and thus Cheong does not anticipate claim 29. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "an apparatus for self-initiated processor instruction issuing including an issue queue, said issue queue comprising a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value" as recited in claim 38. The Examiner cites element 1219 of Cheong as disclosing an issue queue. Paper No. 5, page 7. The Examiner further cites Figure 3; elements 100, 118, 120, 128a, 128b; column 10, lines 48-51; column 11, lines 4-21 and 27-34 of Cheong as disclosing the remaining elements in the above-cited claim limitations. Paper No. 5, page 7. Applicants respectfully traverse.

Cheong instead discloses that Figure 3 depicts a table for tracking the source data required by a dispatched instruction. Column 10, lines 48-49. Cheong further discloses that on dispatch, the dispatch unit passes instruction data into an entry in the PEQ. Column 11, lines 4-5. Cheong further discloses that the source needed bit for source block one is set, and the source needed bit for source block two is low. Column 11, lines 29-31. There is no language in the cited passages that discloses an issue queue (Examiner asserts that instruction queue 1219 discloses the issue queue) that includes a plurality of entries where each entry is operable for containing information associated with an instruction to be issued. Applicants respectfully request the Examiner to explain the connection between instruction queue 1219 and Figure 3 pursuant to 37 C.F.R. §1.104(c)(2). Further, there is no language in the cited passages that discloses an issue queue (Examiner asserts that instruction queue 1219 discloses the issue queue) that includes a plurality of entries where each entry includes a first portion for storing an instruction operand. Applicants respectfully request the Examiner to particularly point out in Cheong where Cheong discloses a first portion that stores an instruction operand pursuant to 37 C.F.R. §1.104(c)(2). Further, there is no language in the cited passages that discloses an issue queue (Examiner asserts that instruction queue 1219 discloses the issue queue) that includes a plurality of entries where each entry includes a second portion for storing a link value. Again, Applicants respectfully request the Examiner to particularly point out in Cheong where Cheong discloses a second portion for storing a link value pursuant

to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 38, and thus Cheong does not anticipate claim 38. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein the second portion comprises a link mask and the link value indicates to a target instruction which of the issue queue's plurality of entries that a dispatching dependent instruction will occupy" as recited in claim 38. The Examiner has not addressed this limitation. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 38. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value corresponding to a number of said first entry" as recited in claim 38. The Examiner cites column 2, lines 32-65; column 9, lines 48-65 and column 15, lines 4-35 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 7. Applicants respectfully traverse and assert that Cheong instead discloses that the processing of one instruction may depend on a result from another instruction. Column 2, lines 32-34. Cheong further discloses that each entry in the GPR table consists of four fields. Column 9, lines 48-49. Cheong further discloses that the first field is the valid/tagged field 100 which has two permissible values, valid and tagged. Column 9, lines 49-51. Cheong further discloses that instruction 2, having TID 2, is now dispatched and the dispatch pointer moved to instruction 3. Column 15, lines 4-6. There is no language in the cited passages that discloses an instruction corresponding to a first entry having a value of the instruction operand determined by an instruction corresponding to a second entry. Neither is there any language in the cited passage that discloses a link value in the second entry. Neither is there any language in the cited passage that discloses a link value in the second

entry comprises a value corresponding to a number of the first entry. Thus, Cheong does not disclose all of the limitations of claim 38, and thus Cheong does not anticipate claim 38. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "setting a predetermined value in a first portion of an entry in an instruction queue corresponding to a first instruction in response to a dispatch of a second instruction" as recited in claim 45. The Examiner cites column 15, lines 4-35 and column 20, lines 21-25 and 37-48 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 9. Applicants respectfully traverse and assert that Cheong instead discloses that instruction 2, having TID 2, is now dispatched and the dispatch pointer moved to instruction 3. Column 15, lines 4-6. Cheong further discloses that Figures 6J-9J provide another illustration where it is assumed that instruction 2 is correctly predicted, the load occurs before the store has reached cache, and the load-hit-store condition is detected before the branch is resolved. Column 20, lines 37-40. There is no language in the cited passages that discloses setting a predetermined value in a first portion of an entry in an instruction queue. Neither is there any language in the cited passages that discloses setting a predetermined value in a first portion of an entry in an instruction queue corresponding to a first instruction in response to a dispatch of a second instruction. Thus, Cheong does not disclose all of the limitations of claim 45, and thus Cheong does not anticipate claim 45. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "writing said predetermined value in a second portion of an entry in said instruction queue corresponding to said second instruction in response to an issuing of said first instruction, wherein a target of said first instruction comprises a source operand of said second instruction" as recited in claim 45. The Examiner cites column 17, lines 15-23 and column 19, lines 50-58 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 9. Applicants respectfully traverse and assert that Cheong instead discloses the PEQ field after dispatch of instruction 6. Column 17, lines 15-23. Cheong further discloses that since the results of instruction 1 are required by instruction 4, which is stored in entry 804 of the PEQ, the PEQ snoops

the result busses and will update the source blocks of entry 804 when it detects the result of instruction 1 on one of the result busses. Column 19, lines 49-54. There is no language in the cited passages that discloses writing a predetermined value in a second portion of an entry in the instruction queue. Neither is there any language in the cited passages that discloses writing a predetermined value in a second portion of an entry in the instruction queue corresponding to the second instruction. Neither is there any language in the cited passages that discloses writing a predetermined value in a second portion of an entry in the instruction queue corresponding to the second instruction in response to an issuing of the first instruction. Neither is there any language in the cited passages that discloses a target of the first instruction comprises a source operand of the second instruction. Thus, Cheong does not disclose all of the limitations of claim 45, and thus Cheong does not anticipate claim 45. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "each execution unit including an apparatus for issuing instructions for execution, said apparatus operable for receiving instructions from said dispatch unit, the apparatus for issuing instructions comprising an issue queue, said issue queue including a plurality of entries, each entry of said plurality operable for containing information associated with an instruction to be issued, wherein each entry includes a first portion for storing an instruction operand and a second portion for storing a link value" as recited in claim 48 for at least the reasons stated above.

Applicants further assert that Cheong does not disclose "wherein the second portion comprises a link mask and the link value indicates to a target instruction which of the issue queue's plurality of entries that a dispatching dependent instruction will occupy" as recited in claim 48. The Examiner cites elements 118, 128a, 128b, 126a, 126b; column 8, lines 23-62 and column 11, lines 31-45 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 9. Applicants respectfully traverse and assert that Cheong instead discloses that the processor is provided with a target identification ("TID") generator which generates tokens or tags, each of which is uniquely associated with an instruction upon dispatch. Column

8, lines 31-34. Cheong further discloses that if the valid/tagged field 124a indicates that the data in valid field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. Column 11, lines 31-34. Cheong further discloses that in the illustrative embodiment of the invention, the execution unit broadcast their results along with the TID of the instruction which generated them. Column 11, lines 38-40. Cheong further discloses that when a TID being broadcast matches the TID value in the source TID field 128a, the GPR value being broadcast is copied into value field 126a and the valid/tagged field 124a is set to indicate valid. Column 11, lines 40-44. There is no language in the cited passages that discloses a second portion that comprises a link mask. Neither is there any language in the cited passages that discloses a second portion that comprises a link mask and a link value. Neither is there any language in the cited passages that discloses a second portion that comprises a link mask and a link value indicates to a target instruction which of the issue queue's plurality of entries that a dispatching dependent instruction will occupy. Thus, Cheong does not disclose all of the limitations of claim 48, and thus Cheong does not anticipate claim 48. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein, for an instruction corresponding to a first entry having a value of said instruction operand determined by an instruction corresponding to a second entry, said link value in said second entry comprises a value representing said first entry" as recited in claim 48 for at least the reasons stated above.

Claims 15-17, 19, 25-28 each recite combinations of features of claim 14, and hence are not anticipated by Cheong for at least the reasons that claim 14 is not anticipated by Cheong. Claims 30-34 each recite combinations of features of claim 29, and hence are not anticipated by Cheong for at least the reasons that claim 29 is not anticipated by Cheong. Claims 39-47 each recite combinations of features of claim 38, and hence are not anticipated by Cheong for at least the reasons that claim 38 is not anticipated by Cheong. Claims 49-52 each recite combinations of features of claim 48, and hence are not anticipated by Cheong for at least the reasons that claim 48 is not anticipated by Cheong. Claims 15-17, 19, 25-28, 30-34, 39-47 and

49-52 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Cheong.

For example, Cheong does not disclose "storing a first queue pointer data value associated with said dispatching instruction in a first portion of an associated rename register entry, said rename register including a plurality of entries, wherein said queue pointer value associates said rename register entry and said preselected queue entry corresponding to said dispatching instruction, and wherein said second queue entry is selected in response to a second queue pointer value" as recited in claim 15. The Examiner cites column 11, lines 4-21; column 14, lines 15-29 and column 16, lines 15-32 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 4. Applicants respectfully traverse and assert that Cheong instead discloses that on dispatch, the dispatch unit passes instruction data into an entry in the PEQ. Column 11, lines 4-5. Cheong further discloses that the TID field 118 contains the TID which was assigned to the dispatched instruction. Column 11, lines 5-6. Cheong further discloses that the valid/tagged field of the history buffer is set to valid, illustrated in the figure by "V", to indicate that the previous instruction which set register 4 has already completed, and the data is available for use by any instruction was issued prior to instruction 1. Column 14, lines 19-23. Cheong further discloses that since instruction 4 is bound for an execution unit associated with the PEQ and an interruptible instruction, entries 804 and 904 are created in the PEQ and interrupt stacks, respectively. Column 16, lines 15-18. There is no language in the cited passages that discloses storing a first queue pointer data value associated with a dispatching instruction. Neither is there any language in the cited passages that discloses storing a first queue pointer data value associated with a dispatching instruction in a first portion of an associated rename register entry. Neither is there any language in the cited passages a rename register including a plurality of entries. Neither is there any language in the cited passages that discloses that the queue pointer value associates the rename register entry and the preselected queue entry corresponding to the dispatching instruction. Neither is there any language in the cited passages that discloses that a second queue entry is selected in response to a second queue pointer value. Applicants respectfully request the Examiner to

particularly point out in the cited passages where these limitations are disclosed pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 15, and thus Cheong does not anticipate claim 15. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "setting said first data value in response to a source operand data value of said dispatching instruction" as recited in claim 16. Applicants further assert that Cheong does not disclose "setting said first data value is omitted in response to a predetermined data value in said first portion of said rename register entry" as recited in claim 17. Applicants further assert that Cheong does not disclose "setting said predetermined data value in said first portion is in response to an issuing of an instruction associated with said second queue entry" as recited in claim 19. Applicants further assert that Cheong does not disclose "wherein said second queue pointer value is associated with a source operand tag of said dispatching instruction" as recited in claim 25. It is unclear whether the Examiner has addressed these limitations. The Examiner appears to be citing column 11, lines 4-21; column 14, lines 15-29 and column 16, lines 15-32 of Cheong as disclosing these limitations; however, the Examiner has not particularly stated where these limitations are disclosed in the cited passages. Upon review of the cited passages, Applicants could not identify any language in Cheong as disclosing any of these limitations. Applicants respectfully request the Examiner to particularly point out where these limitations are disclosed in the cited passages pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claims 16, 17, 19 and 25, and thus Cheong does not anticipate claims 16, 17, 19 and 25. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said second queue pointer value corresponds to a queue entry of an instruction target operand tag matching said source operand" as recited in claim 26. The Examiner cites column 13, line 43 – column 14, line 29 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 4. Applicants respectfully traverse and assert that Cheong instead discloses that once it is determined that sufficient resources exist to dispatch the

instruction, the tables are updated. Column 13, lines 43-44. Cheong further discloses the history buffer after the dispatch of instruction 1. Column 14, lines 15-29. There is no language in the cited passages that discloses a second queue pointer value. Neither is there any language in the cited passages that discloses a second queue pointer value corresponding to a queue entry of an instruction target operand tag matching the source operand. Applicants respectfully request the Examiner to particularly point out where these limitations are disclosed in the cited passages pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 26, and thus Cheong does not anticipate claim 26. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said first data value comprises a link mask having a number of bits equal to a number of entries in said queue" as recited in claim 27. The Examiner cites Figure 5A and column 13, lines 61-64 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 4. Applicants respectfully traverse and assert that Cheong instead discloses that in Figure 5A, the first instruction having TID of 1, has been dispatched and the dispatch point has been moved to instruction 2. Column 13, lines 61-63. There is no language in the cited passage that discloses a first data value comprising a link mask. Neither is there any language in the cited passage that discloses a first data value comprising a link mask having a number of bits equal to a number of entries in a queue. Thus, Cheong does not disclose all of the limitations of claim 27, and thus Cheong does not anticipate claim 27. M.P.E.P. §2131.

Applicants respectfully assert that Cheong does not disclose "setting said predetermined data value is in response to an issuing of an instruction associated with said second queue entry" as recited in claim 28. The Examiner cites column 11, lines 40-45 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 5. Applicants respectfully traverse and assert that Cheong instead discloses that when a TID being broadcast matches the TID value in the source TID field 128a, the GPR value being broadcast is copied into value field 126a and the valid/tagged field 124a is set to indicate valid. Column 11, lines 40-44. There is no language in the cited

passage that discloses that the setting of the predetermined data value is in response to an issuing of an instruction. Neither is there any language in the cited passage that discloses that the setting of the predetermined data value is in response to an issuing of an instruction associated with a second queue entry. Again, the Examiner has not identified which elements discussed in the cited passage disclose any of the above-cited claim limitations. For example, which element allegedly discloses the second queue entry? What is the predetermined value that is being set? How does Cheong show that this predetermined value is being set in response to an issuing of an instruction associated with the second queue entry? Applicants respectfully request the Examiner to particularly point out how the cited passage discloses the above-cited claim limitation pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 28, and thus Cheong does not anticipate claim 28. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein each said rename register device entry includes a third portion operable for receiving a plurality of operand tags, and wherein each said pointer data value is operable for selection in response to a preselected one of said plurality of operand tags" as recited in claim 30. The Examiner cites elements 1233 and 1237 as disclosing a rename register device. Paper No. 5, page 6. The Examiner further cites Figures 1-2 and column 9, lines 37-48 of Cheong as disclosing an entry. Paper No. 5, page 6. The Examiner further cites elements 100 and 112 of Cheong as disclosing a third portion. Paper No. 5, page 6. The Examiner further cites column 8, lines 26-36 and column 9, line 49 – column 10, line 3 of Cheong as disclosing that each pointer data value is operable for selection in response to a preselected one of the plurality of operand tags. Paper No. 5, page 6. Applicants respectfully traverse.

Cheong instead discloses that each entry in the GPR table consists of four fields including the valid/tagged field 100. Column 9, lines 49-50. Cheong further discloses that this field has two permissible values, valid and tagged. Column 9, lines 50-51. Cheong further discloses a history buffer table that includes the valid/tagged field 112. Column 10, lines 15-17. Cheong further discloses that the valid/tagged

field 112 contains data related to the architected register targeted by the dispatched instruction. Column 10, lines 40-42. There is no language in the cited passages that discloses that each rename register device (Examiner cites elements 1233, 1237 as disclosing a rename register device) entry includes a third portion operable for receiving a plurality of operand tags. Fields 100 and 112 of Cheong are not operable for receiving a plurality of operand tags as Applicants understand the Examiner to assert. Neither is there any language in the cited passages that discloses that each pointer data value is operable for selection in response to a preselected one of the plurality of operand tags. Thus, Cheong does not disclose all of the limitations of claim 30, and thus Cheong does not anticipate claim 30. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said queue is operable for broadcasting a preselected first operand tag" as recited in claim 31. The Examiner cites column 11, lines 39-45 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 6. Applicants respectfully traverse and assert that Cheong instead discloses that when a TID being broadcast matches the TID value in the source TID field 128a, the GPR value being broadcast is copied into value field 126a and the valid/tagged field 124a is set to indicate valid. Column 11, lines 40-44. Cheong further discloses that the instruction associated with the entry may then be issued to the appropriate functional unit. Column 11, lines 44-45. There is no language in the cited passage that discloses an instruction queue operable for broadcasting a preselected first operand tag. Thus, Cheong does not disclose all of the limitations of claim 31, and thus Cheong does not anticipate claim 31. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "further comprising a storage device operable for receiving said broadcast first operand tag" as recited in claim 32. The Examiner cites column 5, line 59 – column 6, line 2; column 6, lines 34-40 and 64-67; and column 12, lines 19-31 of Cheong as disclosing the above-cited claim limitations. Paper No. 5, pages 6-7. Applicants respectfully traverse and assert that Cheong instead discloses a data processing system. Column 5, line 59 – column 6, line 2. Cheong further discloses a processor in the data processing system.

Column 6, lines 33-35. Cheong further discloses a sequential fetcher that transmits branch instructions fetched from the instruction cache and the MMU to branch processing unit for execution, but temporarily stores sequential instructions within the instruction queue for execution by other execution circuitry within the processor. Column 6, lines 62-67. Cheong further discloses that the TID field contains the TID of the instruction being dispatched. Column 12, lines 19-20. There is no language in the cited passages that discloses a storage device operable for receiving the broadcast first operand tag. Applicants respectfully request the Examiner to particularly point out in Cheong where Cheong discloses a storage device that receives the broadcast first operand tag pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 32, and thus Cheong does not anticipate claim 32. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said storage device is coupled to said rename register device, and wherein each said rename register device entry includes a fourth portion operable for storing a second data value, said second data value being operable for setting in response to said broadcast first operand tag" as recited in claim 33. The Examiner cites column 9, lines 52-65 and column 12, line 66 – column 13, line 10 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 7. Applicants respectfully traverse and assert that Cheong instead discloses that the valid/tagged field 100 has two permissible values, valid and tagged. Column 9, lines 50-51. Cheong further discloses that this field comprises a single bit which is either high or low depending on the status of the data stored in the second and third fields, the value field 102 and the TID field 104. Column 9, lines 52-55. Cheong further discloses that determining whether sufficient resources are available first involves determining the type of instruction to be dispatched and then checking the appropriate tables for sufficient available entries. Column 12, line 66 – column 13, line 2. Cheong further discloses that instructions which set a GPR require an entry in the PEQ table. Column 13, lines 2-4. There is no language in the cited passage that discloses a storage device coupled to a rename register device (Examiner cites elements 1233 and 1237 of Cheong as disclosing a rename register device). Neither is there any language in the cited passages that

discloses that each rename register device entry (Examiner cites elements 1233 and 1237 of Cheong as disclosing a rename register device) includes a fourth portion operable for storing a second data value where the second data value being operable for setting in response to the broadcast first operand tag. Applicants respectfully request the Examiner to more particularly point out where Cheong discloses a "fourth portion", "a second data value" and "broadcast first operand tag" pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claim 33, and thus Cheong does not anticipate claim 33. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said first data value is operable for setting in response to said second data value" as recited in claim 34. The Examiner cites column 9, lines 52-65 and column 12, line 66 – column 13, line 10 of Cheong as disclosing the above-cited claim limitation. Paper No. 5, page 7. Applicants respectfully traverse and assert that Cheong instead discloses that the valid/tagged field 100 has two permissible values, valid and tagged. Column 9, lines 50-51. Cheong further discloses that this field comprises a single bit which is either high or low depending on the status of the data stored in the second and third fields, the value field 102 and the TID field 104. Column 9, lines 52-55. Cheong further discloses that determining whether sufficient resources are available first involves determining the type of instruction to be dispatched and then checking the appropriate tables for sufficient available entries. Column 12, line 66 – column 13, line 2. Cheong further discloses that instructions which set a GPR require an entry in the PEQ table. Column 13, lines 2-4. There is no language in the cited passages that discloses a first data value operable for setting in response to the second data value. Thus, Cheong does not disclose all of the limitations of claim 34, and thus Cheong does not anticipate claim 34. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein, for said first entry comprising an "*i*th" entry of said plurality of entries, said value representing said first entry is a value of an "*i*th" bit of a plurality of bits of said link value in said second entry" as recited in claim 39 and similarly in claim 49. The Examiner cites Figure 3 and column 10, line 66 – column 11, line 21 of Cheong as disclosing the

above-cited claim limitation. Paper No. 5, page 8. Applicants respectfully traverse and assert that Cheong instead discloses that the PEQ table comprises a plurality of entries. Column 10, lines 66-67. Cheong further discloses that each entry contains nine fields, namely, the TID field 118, the opcode field 120, destination field 122 and two source blocks. Column 10, line 67 – column 11, line 2. There is no language in the cited passage that discloses that for the first entry comprising an "*i*th" entry of the plurality of entries the value representing the first entry is a value of an "*i*th" bit of a plurality of bits of the link value in the second entry. Applicants respectfully request the Examiner to particularly point out in Cheong where Cheong discloses the "first entry", the "*i*th entry", the value representing the first entry, the "*i*th bit", the "link value" and the "second entry" pursuant to 37 C.F.R. §1.104(c)(2). Thus, Cheong does not disclose all of the limitations of claims 39 and 49, and thus Cheong does not anticipate claims 39 and 49. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein each entry of said instruction queue further includes a third portion, and wherein said third portion in said first entry is operable for receiving said link value in said second entry in response to an issuing of said instruction corresponding to said second entry" as recited in claim 40. The Examiner has not addressed this limitation. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 40. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein a data value in said third portion is operable for signaling an operand in a second portion of a corresponding entry of said plurality of entries is ready" as recited in claim 41. The Examiner has cited column 11, lines 27-34 and column 20, line 49 – column 21, line 22 of Cheong as disclosing the above-cited claim limitation. Paper No. 3, page 8. Applicants respectfully traverse and assert that Cheong instead discloses that Cheong

further discloses that to illustrate the operation of the PEQ, it will be assumed that only one source register is required by the instruction associated with the PEQ entry. Column 11, lines 27-29. Cheong further discloses that the source needed bit for source block one is set and the source needed bit source block two is low. Column 11, lines 29-31. Cheong further discloses that if the valid/tagged field 124a indicates that the data in value field 126a is valid, then the instruction stored in the PEQ entry is ready to be issued for execution. Column 11, lines 31-34. Cheong further discloses the operation of the invention in which the instructions execute in the order of 1, 5, 4, 3 and 6, at which time an exception occurs indicating that the store detects that the load should have waited for store data. Column 20, lines 49-53. There is no language in the cited passages that discloses a data value in the third portion is operable for signaling an operand in a second portion of a corresponding entry of the plurality of entries is ready. Thus, Cheong does not disclose all of the limitations of claim 41, and thus Cheong does not anticipate claim 41. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue" as recited in claim 42. The Examiner has not addressed this limitation. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 42. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein each entry of said plurality of entries of said rename unit further includes a second portion operable for storing a pointer to said associated entry of said plurality of entries in said issue

queue" as recited in claim 43. The Examiner has not addressed this limitation. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 43. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein said predetermined value in said first portion of said instruction queue entry is set in response to a validity value corresponding to said source operand, said validity value stored in an entry in a rename unit coupled to said instruction queue" as recited in claim 46. The Examiner has not addressed this limitation. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 46. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "a rename register unit coupled to said issue queue, said rename unit including a plurality of entries, said plurality of entries of said rename unit having a same number of entries as a number of entries of said instruction queue, and wherein each entry has a first portion operable for storing a data value signaling instruction information is stored in an associated entry of said plurality of entries in said issue queue" as recited in claim 50. On page 10 of Paper No. 5, the Examiner misquotes the limitations of claim 50 and therefore has not addressed the limitations of claim 50. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the

Examiner has not established a *prima facie* case of anticipation in rejecting claim 50. M.P.E.P. §2131.

Applicants further assert that Cheong does not disclose "wherein each entry of said plurality of entries of said rename unit further includes a second portion operable for storing a pointer to said associated entry of said plurality of entries in said issue queue" as recited in claim 51. On page 10 of Paper No. 5, the Examiner misquotes the limitations of claim 51 and therefore has not addressed the limitations of claim 51. The Examiner is reminded that the Examiner bears the burden of establishing a *prima facie* case of anticipation which involves identifying a reference that expressly or inherently describes each and every element as set forth in the claim. M.P.E.P. §2131. Since the Examiner has not provided any evidence that Cheong discloses the above-cited claim limitation, the Examiner has not established a *prima facie* case of anticipation in rejecting claim 51. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Cheong, and thus claims 14-17, 19, 25-34, 38-52 are not anticipated by Cheong. M.P.E.P. §2131.

II. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 10-17, 19, 25-34 and 38-52 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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